**Office of the Dean Research and Consultancy**
**Indian Institute of Engineering Science & Technology (IIEST), Shibpur**
**Howrah-711 103**

**Project on: "Design and Development of SoC for Industry 4.0 with Functional safety and security"**

**[Sponsoring Authority: Chip to Startup (C2S), MeitY, Govt. of India]**

**School of VLSI Technology**
**Indian Institute of Engineering Science & Technology (IIEST), Shibpur**
**Howrah-711 103**

**Ref: Advt. No. VL 1826, published in the "Statesman (All Editions)" dated 16.10.2023**

**[University Project Code: DRC/MEITY-C2S (4197)/VLSI/HR/005/23-24]**

Interested candidates are requested to appear for walk-in interview on 17.11.2023 at 11:00 AM for the following post in the School of VLSI Technology Department, **Indian Institute of Engineering Science & Technology (IIEST), Shibpur, Howrah-711 103**.

**Name of the post: Senior Project Associate (1 no.)**

**No of post–** One

**Essential Qualification**: Ph.D. in VLSI design or related discipline / M. Tech having 3 years of experience in Analog and Mixed Signal Design and research paper publication with 65% marks or 7.0 CGPA along with Institute norms.

**Fellowship**: INR 54,000 per month (10% increment each year subject to satisfactory performance)(consolidated).

**Age Limit:** Maximum 35 years, (Upper age limit is relaxable up to 5 years for SC/ST/OBC/Woman and Physically handicapped candidates).

**Name of the post: Project Associate – II (1no.)**

**No of post–** One

**Essential Qualification**: M. Tech with domain knowledge in VLSI design and research paper publication with 65% marks or 7.0 CGPA and Institute norms.

**Fellowship**: INR 45,000 per month (10% increment each year subject to satisfactory performance) (consolidated).

**Age Limit:** Maximum 32 years (Upper age limit is relaxableup to 5 years for SC/ST/OBC/Woman and Physically handicapped candidates).

**Desirable Qualification (s):**
Experience with Analog and Mixed Signal Design, FPGA, Coding, chip tape-out and IC testing. Applicants with a GATE score will be preferable.

**Experience / Software / Skillset:**
Experience in Analog and Mixed Signal Design, Design knowledge of low power design, knowledge of RISC-V, experience in chip tape out, product design, and testing. Knowledge of VLSI EDA Tools, Verilog, RTL coding, and Functional Coding using C, Verilog-A and MATLAB.

**Job Descriptions:**
- ✓ Carry out research in IC design, testing, and product development for Industry 4.0.
- ✓ Coordinate with cluster institutes for project activities and attend training.
- ✓ Maintain EDA tools and laboratory workstations and support students in the related area.
- ✓ Create essential documentation for projects and manuals for EDA tools.

- ✓ Assisting PIs with various activities towards completion of the project.

**Applicants (with M. Tech) are expected to pursue a Ph.D. in School of VLSI Technology, satisfying the Institute Eligibility Criteria.**

**Duration**: 5 years or until the completion of the project, subject to yearly evaluation of the candidate for the project execution.

Interested eligible candidates should mail soft copies of the application letter in plain paper, recent bio-data, mark sheets, certificates research papers (if any), work experience certificate (if any), etc., in a single PDF file sent by email with "Advertisement No." on the subject link to the below-mentioned e-mail ID. All documents should be self-attested. Physical documents will be verified at the time of joining. The selection will be cancelled if any discrepancies are found in the documents at the time of physical verification.

**Venue of the interview**: School of VLSI Technology Department, IIEST, Shibpur.

**Note:**

1. Soft copies of the application letter, bio-data, mark sheets and certificates should be sent through e-mail in advance by November 10, 2023 at 5:00 pm to: Prof. Hafizur Rahaman, Project Investigator (E-mail id: hafizur@vlsi.iiests.ac.in).
2. All applications must mention a valid e-mail id and phone number for communicating date of interview.
3. Short listing may be done before the interview.

**Dean (R & C)**

**(W. Code DRC-004/23-24)**